IN THE CLAIMS

Please cancel claims 12-13, and 21.

Please amend claims 1, 9 and 18 as indicated below.

1. (Currently Amended) A method for generating a plurality of clock frequencies over a period of time in a linear manner, said method comprising:
generating a first clock signal with a first frequency; and
counting sequences of pulses of said first clock signal, wherein said sequences include a fixed number of pulses;
utilizing said first clock signal to generate a second clock signal;
wherein said second clock signal is generated with a plurality of clock frequencies, said plurality of clock frequencies including a beginning clock frequency, one or more intermediate clock frequencies, and an ending clock frequency; and
wherein a transition from said beginning clock frequency, through said intermediate clock frequencies, to said ending clock frequency is performed in a linear manner by dropping selected pulses of said first clock signal; and
detecting said selected pulses of said first clock signal, wherein said selected pulses correspond to particular counts of said pulses within said fixed number of pulses.

2. (Original) The method of claim 1, wherein utilizing said first clock signal comprises using said first clock signal to select a sequence of values from a storage element.

3. (Original) The method of claim 2, wherein said storage element comprises a first and second shift register, and wherein said sequence of values are alternately selected from said registers.

4. (Previously Presented) The method of claim 1, wherein performing said transition comprises either dropping a successively greater number of pulses or dropping a successively fewer number of pulses.

5. (Canceled).

6. (Original) The method of claim 3, further comprising loading said shift registers with predetermined values.

7. (Previously Presented) The method of claim 6, further comprising changing a contents of said shift registers at selected times in order to generate said second clock signal with an increasing frequency.

8. (Previously Presented) The method of claim 6, further comprising changing a contents of said shift registers at selected times in order to generate said second clock signal with an decreasing frequency.

9. (Currently Amended) A clock circuit for generating a plurality of clock frequencies over a period of time in a linear manner, the clock circuit comprising:

a first circuit configured to generate a first clock signal; ~~and~~

a counter configured to count sequences of pulses of said first clock signal, wherein said sequences include a fixed number of pulses; and

circuitry configured to utilize said first clock signal to generate a second clock signal;

wherein said second clock signal is generated with a plurality of clock frequencies, said plurality of clock frequencies including a beginning clock frequency, one or more intermediate clock frequencies, and an ending clock frequency; ~~and~~

wherein a transition from said beginning clock frequency, through said intermediate clock frequencies, to said ending clock frequency is

performed in a linear manner by dropping selected pulses of said first clock signal; and

wherein said circuitry is configured to detect said selected pulses of said first clock signal, wherein said selected pulses correspond to particular counts of said pulses within said fixed number of pulses.

10. (Original) The clock circuit of claim 9, further comprising a storage element configured to store a pattern of bits, wherein said circuitry is configured to utilize said first clock signal to select a sequence of values from a storage element.

11. (Original) The clock circuit of claim 10, wherein said storage element comprises a first and second shift register, and wherein said circuitry is configured to select said sequence of values from said registers in an alternating manner.

12. (Canceled).

13. (Canceled).

14. (Original) The clock circuit of claim 11, wherein said first circuit is further configured to load said shift registers with predetermined values.

15. (Original) The clock circuit of claim 14, wherein said first circuit is further configured to change a contents of said shift registers at selected times in order to generate said second clock signal with an increasing frequency.

16. (Original) The clock circuit of claim 14, wherein said first circuit is further configured to change a contents of said shift registers at selected times in order to generate said second clock signal with a decreasing frequency.

17. (Original) The clock circuit of claim 9, wherein said clock circuit is included within a processor.

18. (Currently Amended) A system comprising:

a reference clock generator configured to generate a reference clock signal; and

a processor comprising a clock circuit configured to:

receive said reference clock signal;

count sequences of pulses of said first clock signal, wherein said sequences include a fixed number of pulses;

generate a first clock signal from said reference clock signal; and

utilize said first clock signal to generate a second clock signal;

wherein said second clock signal is generated with a plurality of clock frequencies, said plurality of clock frequencies including a beginning clock frequency, one or more intermediate clock frequencies, and an ending clock frequency; and

wherein a transition from said beginning clock frequency, through said intermediate clock frequencies, to said ending clock frequency is performed in a linear manner by dropping selected pulses of said first clock signal; and

detect said selected pulses of said first clock signal, wherein said selected pulses correspond to particular counts of said pulses within said fixed number of pulses.

19. (Original) The system of claim 18, further comprising a storage element configured to store a pattern of bits, wherein said clock circuit is configured to utilize said first clock signal to select a sequence of values from a storage element.

20. (Original) The system of claim 19, wherein said storage element comprises a first and second shift register, and wherein said clock circuit is configured to select said sequence of values from said registers in an alternating manner.

21. (Canceled).

22. (Original) The system of claim 20, wherein said clock circuit is further configured to load said shift registers with predetermined values.

23. (Original) The system of claim 22, wherein said clock circuit is further configured to change a contents of said shift registers at selected times in order to generate said second clock signal with an increasing frequency.

24. (Original) The system of claim 22, wherein said clock circuit is further configured to change a contents of said shift registers at selected times in order to generate said second clock signal with a decreasing frequency.

25. (Original) The system of claim 18, further comprising a system controller coupled to said processor, wherein said system controller is coupled to receive said reference clock signal.

26. (Original) The system of claim 25, wherein said system controller is further coupled to a main memory, graphics adapter, and peripheral bus controller.